

AD-A035 266

ARMY ELECTRONICS COMMAND FORT MONMOUTH N J

F/G 20/12

LOW TEMPERATURE PRESSURE-OXIDATION OF SILICON FOR INTEGRATED CI--ETC(U)

JAN 77 R J ZETO, C G THORNTON, E HRYCKOWIAN

UNCLASSIFIED

ECOM-4459

NL

1 OF 1  
AD-A  
035 266



END  
DATE  
FILMED  
3-8-77  
NTIS

U.S. DEPARTMENT OF COMMERCE  
National Technical Information Service

AD-A035 266

LOW TEMPERATURE PRESSURE-OXIDATION OF SILICON  
FOR INTEGRATED CIRCUIT TECHNOLOGY

ARMY ELECTRONICS COMMAND  
FORT MONMOUTH, NEW JERSEY

JANUARY 1977

ADA 035266



Research and Development Technical Report

ECOM -4459

LOW TEMPERATURE PRESSURE-OXIDATION OF SILICON FOR  
INTEGRATED CIRCUIT TECHNOLOGY

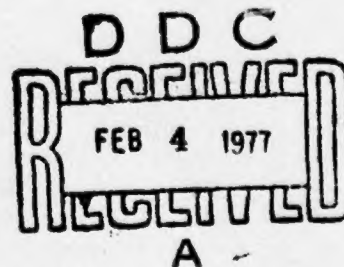
R. J. Zeto  
C. G. Thornton  
E. Hryckowian  
C. D. Bosco

Electronics Technology & Devices Laboratory

January 1977

DISTRIBUTION STATEMENT

Approved for public release;  
distribution unlimited.



**ECOM**

REPRODUCED BY  
NATIONAL TECHNICAL  
INFORMATION SERVICE  
U. S. DEPARTMENT OF COMMERCE  
SPRINGFIELD, VA. 22161

US ARMY ELECTRONICS COMMAND FORT MONMOUTH, NEW JERSEY 07703

## NOTICES

### Disclaimers

The findings in this report are not to be construed as an official Department of the Army position, unless so designated by other authorized documents.

The citation of trade names and names of manufacturers in this report is not to be construed as official Government indorsement or approval of commercial products or services referenced herein.

### Disposition

Destroy this report when it is no longer needed. Do not return it to the originator.

DATE	FILED	<input checked="checked" type="checkbox"/>
DATE	FILED	<input type="checkbox"/>
EXEMPTION		
BY		
DISTRIBUTION/AVAILABILITY CODES		
1	2	3
4	5	6
7	8	9
10	11	12



REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER ECOM-4459	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) Low Temperature Pressure-Oxidation of Silicon for Integrated Circuit Technology		5. TYPE OF REPORT & PERIOD COVERED
7. AUTHOR(s) Robert J. Zeto Eugene Hryckowian Clarence G. Thornton Charles D. Bosco		6. PERFORMING ORG. REPORT NUMBER
9. PERFORMING ORGANIZATION NAME AND ADDRESS Electronic Materials Research Technical Area US Army Electronics Technology & Devices Lab (ECOM) Fort Monmouth, NJ 07703 DRSEL-TL-ES		8. CONTRACT OR GRANT NUMBER(s)
11. CONTROLLING OFFICE NAME AND ADDRESS US Army Electronics Command Fort Monmouth, NJ 07703 DRSEL-TL-ES		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 61101A 1T161101A91A 09 427 61102A 1L161102AH47 S7 021
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)		12. REPORT DATE January 1977
		13. NUMBER OF PAGES 13
		15. SECURITY CLASS. (of this report) Unclassified
		16a. DECLASSIFICATION/DOWNGRADING SCHEDULE
16. DISTRIBUTION STATEMENT (of this Report)  Approved for public release; distribution unlimited.		
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)		
18. SUPPLEMENTARY NOTES  This paper was presented at the 10th Army Science Conference, US Army Military Academy, West Point, NY, 23 June 1976. Published in the Proceedings.		
19. KEY WORDS (Continue on reverse side if necessary and identify by block number) Silicon MOS Properties Semiconductor Integrated Circuits Passivation Oxide Isolation Oxygen Pressure Oxidation		
20. ABSTRACT (Continue on reverse side if necessary and identify by block number) A research study of the effect of dry oxygen pressure on the thermal oxidation of silicon has resulted in a new passivation technique that is expected to improve the performance, cost and reliability of large scale integrated circuit devices. Based on existing theory of the oxidation mechanism, it was reasoned that dry oxygen pressures above 1 atm would appreciably accelerate the oxidation of silicon, thereby leading to lower oxidation temperatures, reduced defect concentrations, and improved electrical properties. Special apparatus has been		

Cont'd

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE(When Data Entered)

20. Abstract (cont'd)

developed, and careful experimentation has demonstrated that oxidation temperatures can be lowered as much as 400°C by using only 140 atm dry oxygen pressure, i.e., a pressure lower than that contained in commercial bottled gas cylinders. Measurements have shown that the resultant oxidized material has a stable flat-band voltage, consistently low fixed surface-state-charge density, high dielectric strength, and a generally lower defect concentration relative to conventionally processed silicon. The use of pressure-oxidation (P-OX) to obtain oxide-isolated integrated circuits on sapphire to meet military requirements for low power and radiation hardening was demonstrated. The research technique is being applied by ECOM microelectronics engineers, and several industrial concerns have indicated plans for using this process. Suitable P-OX equipment on a production scale is being designed under DARPA sponsorship.

1a

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE(When Data Entered)



## CONTENTS

	<u>Page</u>
INTRODUCTION	1
BACKGROUND	2
EXPERIMENTAL	4
RESULTS	5
OXIDE-ISOLATED INTEGRATED CIRCUITS	9
FUTURE PLANS	11
CONCLUSIONS	11
ACKNOWLEDGMENTS	12
REFERENCES	13

## FIGURES

1. Pressure-oxidation of (111) silicon at 800°C, 140 atm dry oxygen compared with other methods: (a) 1 atm dry oxidation at 800°C; (b) 1 atm steam oxidation at 800°C; and (c) 1 atm dry oxidation at 1200°C 6
2. Influence of pressure and temperature on oxide growth for 3-hour oxidations of (111) silicon 7
3. Dry pressure-oxidation of nitride on 1 micrometer (100) SOS structure showing 2.2 micrometer pressure-oxide (light) and masking nitride (dark) with complete oxide-isolation between the silicon areas under the nitride 10

LOW TEMPERATURE PRESSURE-OXIDATION OF SILICON  
FOR INTEGRATED CIRCUIT TECHNOLOGY

ROBERT J. ZETO, PhD, CLARENCE G. THORNTON, PhD  
EUGENE HRYCKOWIAN, MR., AND CHARLES D. BOSCO, MR.  
USA ELECTRONICS TECHNOLOGY AND DEVICES LABORATORY (ECOM)  
FORT MONMOUTH, NEW JERSEY 07703

INTRODUCTION

It is widely recognized that the cost, reliability, and performance of large scale integrated (LSI) circuit devices are adversely affected by the large number of process-induced chemical and physical defects that result from high processing temperatures in the range 950 to 1250°C. This impact is particularly severe in the case of oxide-isolated processes and silicon-on-sapphire (SOS) technology as used to produce specialized military devices for low-power, high density, and radiation hardened applications. Consequently, there is strong motivation for developing an oxidation process that can produce gate, field, and other masking and passivating oxides at lower processing temperatures for silicon integrated circuit devices. Such a process has resulted from research on the pressure-oxidation (P-OX) of silicon as conducted at the Electronics Technology and Devices Laboratory of ECOM (1).

It will be shown that the thermal oxidation of silicon is significantly accelerated by elevated, but practical, dry oxygen pressures, with substantial reductions in oxidation temperatures and times. Specialized oxygen gas pressure apparatus suitable for high purity semiconductor research was developed; oxide growth was explored for the regimes 600 to 900°C and 75 to 500 atmospheres (atm); the oxidation mechanism was examined; the dielectric and electronic interface properties were measured; and the technique was applied to integrated circuit (IC) structures. Oxidation temperatures are lowered as much as 400°C by using only 140 atm (2060 psi) dry oxygen



pressure, and the physical and electronic properties of the oxide are equal or superior to those obtained by conventional means. Currently, P-OX is being incorporated into silicon-on-sapphire (SOS) IC device fabrication in a joint research/device program, and a P-OX system for industrial utilization in IC processing is being designed under ARPA sponsorship. On the basis of the scientific knowledge gained with silicon, it is further anticipated that analogous benefits can be achieved to overcome another serious barrier problem in electronics technology, namely, the passivation of III-V semiconductors.

#### BACKGROUND

The thermal oxidation of silicon is an essential step that is involved in the fabrication of almost all ICs. The oxide layer on silicon is conventionally formed by thermal oxidation at temperatures in the range of 950 to 1250°C with an oxidizing medium of dry or wet oxygen gas at 1 atm. Dry oxides are, in general, preferred when oxide perfection is at a premium, i.e., in a gate region of a metal-oxide-semiconductor (MOS) device. Typical conditions for the formation of a dry gate oxide on silicon are a 4-hour oxidation at 1000°C using an oxidizing medium of 1 atm dry oxygen gas. Wet oxidation is currently needed and used, however, when thick field oxides are required, since wet oxidation of silicon proceeds at a faster rate than dry oxidation. The preparation of a typical 1.5 micrometer field oxide, for example, requires about a 51-hour oxidation at 1200°C by dry oxygen but only about a 3-hour oxidation at 1200°C by wet oxygen. Nevertheless, at lower temperatures such as 1000°C, 1 atm wet oxidation still requires oxidation times in the range of 10 to 15 hours to achieve the oxide thicknesses of 1.5 to 2 micrometers required for oxide-isolation processes. Wet oxidation consists of either 1 atm steam or 1 atm oxygen gas that has been bubbled through water preheated at about 90 to 95°C.

Several different kinds of problems exist with the present high temperature processes, all of which would be ameliorated or eliminated by low temperature processing. For example, the stress introduced due to radial temperature gradients and differences in coefficients of expansion in the grown layer and the substrate typically produces high defect densities. Contamination from deleterious alkali and heavy metal ions is also a greater problem at higher temperatures and particularly in a wet ambient. Lifetime and resistivity may also be severely degraded, and specific desired impurity distributions achieved in previous processing steps may be destroyed by high temperature diffusion during oxidation. All of these deleterious effects serve to severely limit the yield of resultant devices.

Reduction of defects is also desirable to permit realization of advanced devices; for example, high dielectric strength is needed for very thin oxides of about 0.01 to 0.05 micrometers in thickness for short-channel high-transconductance MOS transistors for high speed MOS circuits.

Two existing methods for the preparation of silicon dioxide at reduced temperatures involve chemical vapor deposition (CVD) and high pressure steam. The disadvantage of the CVD method is the fact that the silicon/silicon-dioxide interface properties of deposited oxides are inferior to those of thermally grown oxides. High pressure steam permits oxide growth at reduced oxidation temperatures and times (2), but the stringent oxide and electrical interface characteristics required for LSI devices have not been reported and the method is not generally used.

On the basis of the authors' previous experience in high pressure chemistry, the use of dry oxygen pressures above 1 atm appeared particularly logical and promising for achieving lower thermal oxidation temperatures, reduced defect concentrations, and improved electrical properties in terms of the above state-of-the-art of integrated electronics technology. According to the model of Deal & Grove (3), the growth of oxide films greater than about 230 Å on silicon takes place in the following three stages: (1) transfer of oxidant from the oxidizing gas to the oxide surface, (2) transport of the oxidant across the oxide film towards silicon, and (3) chemical reaction of the oxidant with silicon. The overall oxidation process is mathematically described by the mixed linear-parabolic expression

$$x^2 + Ax = B(t + \tau) \quad (1)$$

where  $x$  is the oxide thickness at time  $t$ ,  $B$  is the parabolic rate constant,  $B/A$  is the linear rate constant, and  $\tau$  is a constant accounting for the presence of the initial oxide layer. The parabolic rate constant is proportional to the partial pressure of the oxidizing species in the gas, thus it was evident that pressures above 1 atm would serve to accelerate the oxide growth rate. On the basis of the 1 atm oxidation mechanism, a theoretical oxide growth curve of thickness versus time was calculated for 800°C, 150 atm to determine the magnitude of the pressure effect that might be expected in terms of a reduction of oxidation temperature. These calculations revealed that if the 1 atm oxidation mechanism persisted to higher pressures, 150 atm dry oxygen pressure would yield equivalent growth rates with

over a 400°C reduction of oxidation temperature from 1200°C, 1 atm oxidation, a significant benefit well worth pursuing.

A search of the scientific literature revealed no data for the dry oxidation of silicon at oxygen pressures above 1 atm. Also, no such data was known to other knowledgeable scientists (4,5) working in this field. Nevertheless, the overall technical community expressed great interest in the proposed research and attached considerable importance to the possible results. Several reasons for the absence of this data were determined to be concern over the potential hazard of working with high pressure oxygen and lack of suitable equipment and experience within the existing electronics industry. For a number of years, the Electronics Technology and Devices Laboratory of ECOM has actively investigated pressure effects on the physics and chemistry of solids. In fact, recent research studied the improvement of dielectric properties, particularly dielectric strength, of a glass/ceramic niobate crystallized under oxygen pressure, which was reported at the 1972 Army Science Conference (6). With this experience and knowledge in pressure technology, a research program was initiated to experimentally investigate the oxidation kinetics and mechanism of the thermal oxidation of silicon at dry oxygen pressures above 1 atm.

#### EXPERIMENTAL

The thermal oxidation of silicon is conventionally conducted in a dynamic condition of flowing oxygen gas, whereas P-OX must be a static oxidation by its very nature. This distinction mandated several important modifications from the conventional method of silicon oxidation. A vacuum system had to be incorporated into the apparatus to control ambient atmosphere in the vessel after samples were loaded into the vessel at room conditions. Procedures had to be conceived not only for all aspects of the pressure-oxidation itself (such as heating, cooling, annealing), but also for controlling the presence of water vapor in the oxidizing gas. Also, stringent cleanliness criteria unique to semiconductor processing had to be observed in the overall development of apparatus and procedures. For example, the presence of sodium contamination in the amount of a few parts per billion at any point in the process would have rendered the oxides unusable for device application.

The P-OX apparatus was basically a converted system originally designed for hydrothermal crystal growth. The water pump was replaced with an oxygen pump; a vacuum pump with cold trap and oil filter was incorporated; and a Panametrics hygrometer was installed.



High purity (99.998%) dry oxygen gas (less than 3 parts per million water vapor and less than 1 part per million hydrocarbons as methane) from a conventional bottled gas cylinder was used to charge the oxygen pump with a Precision Gas Products high pressure gas filter for 0.3 micrometer particles. The stainless steel pressure lines were enlarged where necessary for vacuum operations and pressure gages specially cleaned for oxygen service were used. The pressure vessel was a cold-seal cone-in-cone type heated by an external resistance furnace. Samples were positioned in a quartz sample holder at the bottom of a quartz tube that loosely approximated the inside of the vessel. All quartz was Amersil T08 grade for semiconductor purity. Samples were prepared for oxidation by a 20-minute bath in a mixture of sulfuric and nitric acids (2:1) at 85°C followed by a deionized water rinse and a 45-second dip in 5% hydrofluoric acid. After again rinsing in deionized water, the samples were blown dry with nitrogen gas and immediately loaded in the quartz sample holder and tube. Special attention was given to the potential role of water vapor. In situ hygrometer measurements verified that the oxidations were conducted with less than 14 ppm water vapor at the conclusion of an experiment, and that the observed oxide growth data were truly due to the effect of dry oxygen pressure rather than a catalytic effect of moisture (1). Temperature and pressure were maintained within  $\pm 2^\circ\text{C}$  and  $\pm 10$  atm, respectively, during the course of the oxidations. Oxide thickness was measured with a Rudolph RR100 ellipsometer. The overall uncertainty in thickness ranged from  $\pm 20 \text{ \AA}$  for thin oxides to a maximum of  $\pm 200 \text{ \AA}$  for some of the thicker oxides.

## RESULTS

The rate of oxidation of arsenic-doped (111) silicon at 800°C, 140 atm dry oxygen pressure was measured and compared with conventional (3,7) thermal oxidation methods. The results are shown in Figure 1. It is evident that oxide growth by 140 atm dry P-OX is faster than either 1 atm dry oxidation (curve a) or 1 atm wet oxidation (curve b) at 800°C. Most significant, however, is the fact that oxide growth by 140 atm dry P-OX at 800°C is comparable to 1200°C dry oxidation at 1 atm (curve c). The 400°C reduction in dry oxidation temperature was achieved by the application of only 140 atm pressure (2060 psi), which is less than that contained in conventional pressurized gas cylinders that are widely used and ordinarily handled. Thus the technique is expected to be amenable to practical utilization.

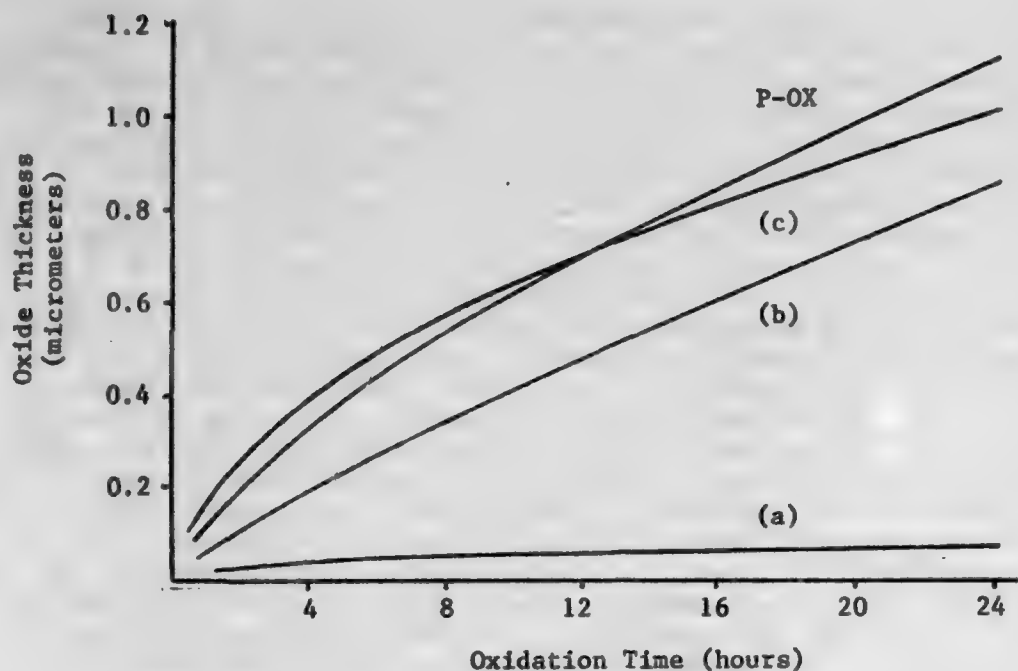


Figure 1. Pressure-oxidation of (111) silicon at 800°C, 140 atm dry oxygen compared with other methods: (a) 1 atm dry oxidation at 800°C; (b) 1 atm steam oxidation at 800°C; and (c) 1 atm dry oxidation at 1200°C.

The crossover of the P-OX data with curve (c) in Figure 1 suggests an altered oxidation mechanism by oxygen pressures above 1 atm. According to the model of Deal & Grove (3), the thermal oxidation of silicon is initially reaction-rate limited at the oxide-silicon interface followed by diffusion control of the oxidant through the oxide. The coefficients in the oxidation equation (1) were determined for the P-OX data and were compared to the corresponding coefficients for 1 atm oxidation at 800°C. Both the parabolic and linear rate constants are one to two orders of magnitude larger for 140 atm dry oxidation, indicating that both of these stages of the oxidation process are accelerated by pressures above 1 atm. The pressure variation of the coefficients, however, indicates that the pressure-oxidation mechanism is not completely described by the model. The coefficient  $A$  is not independent of pressure, and neither the parabolic nor the linear rate constants are proportional to pressure. This is also reflected by the fact that the experimental thickness versus time

oxide growth is lower than that calculated according to equation (1) using 1 atm rate constants. Additional oxide growth rate curves are being determined as a function of pressure and temperature to elucidate the pressure-oxidation mechanism of silicon.

From the data in Figure 1, it is evident that a standard gate oxide of 1200 Å on (111) silicon can be grown in about 1 hour at 800°C, 140 atm. Experiments with (100) silicon showed that a similar gate oxide could be grown in about 2 hours at the same conditions. To explore the breadth of dry pressure-oxidation of silicon in terms of oxides available from various pressures and temperatures, particularly for field or isolation oxides, exploratory 3-hour oxidations of (111) silicon were conducted at pressures in the range 75 to 500 atm and temperatures in the range 700 to 900°C. The results are shown in Figure 2.

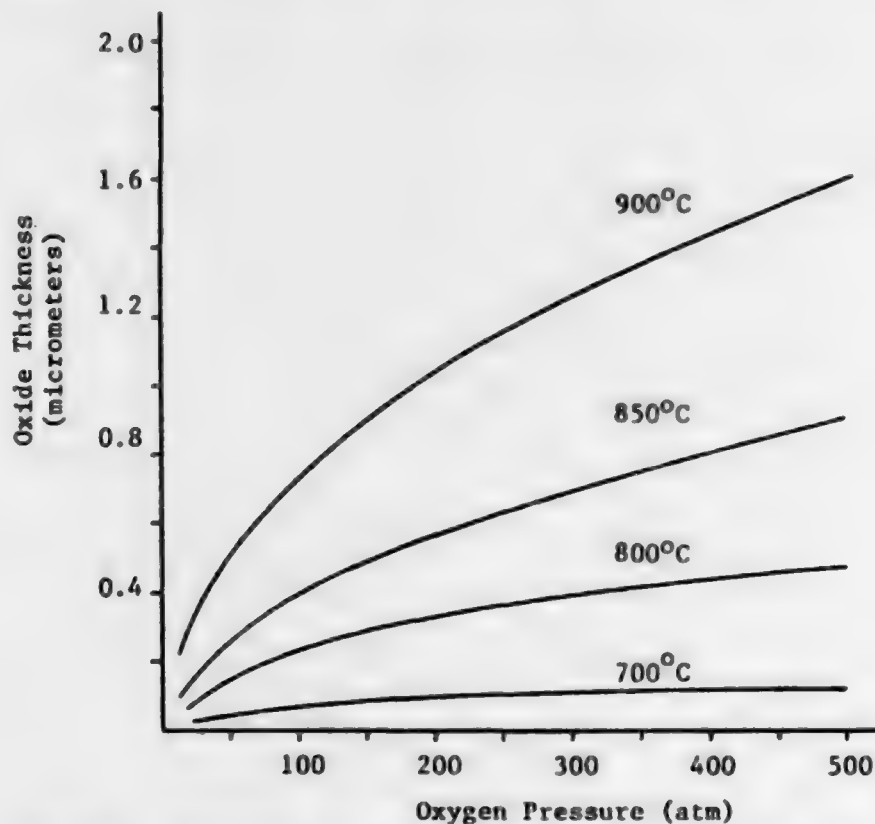


Figure 2. Influence of pressure and temperature on oxide growth for 3-hour oxidations of (111) silicon.



Of particular interest is the 1.6 micrometer oxide that is obtained in 3 hours by 900°C, 500 atm dry P-OX. We have ascertained that these pressure/temperature conditions can be routinely achieved with an internally heated, externally cooled pressure vessel having virtually infinite lifetime and satisfactory personnel safeguards during operation. Clearly, the dry P-OX technique offers definite advantages in reduced oxidation temperatures and oxidation times for the preparation of gate, field, and isolation oxides encompassing a wide range of integrated circuit devices.

The previous P-OX data were obtained using small rectangular samples (8 x 10 mm) in a 0.5 inch ID vessel. The next step in the investigation was to determine the actual benefits of reduced temperature oxidation in terms of MOS properties. For this purpose a P-OX system was assembled utilizing a 1.3 inch ID vessel for oxidizing 1 inch diameter wafers. The vessel employed a Bridgman type seal for holding gas pressure with the larger vessel bore. Gate oxides of about 1000 Å were prepared on phosphorus-doped (111) silicon by dry P-OX at 800°C, 150 atm. Aluminum dots were evaporated to make MOS capacitors. Conventional capacitance versus voltage measurements on the capacitors showed negligible (less than 0.1 volt) shift in flat-band voltage under bias-temperature stress, values of surface-state-charge density ( $Q_{ss}/q$ ) in the range 3 to  $8 \times 10^{-10} \text{ cm}^{-2}$ , and dielectric strength values of about 20 megavolts/cm. Such values represent an improvement by more than a factor of two over those generally reported in the literature for conventionally grown oxides, but it must be pointed out that these properties resulted from initial experiments and all values await subsequent verification. Nevertheless, it is apparent that significant benefits are transferred to electrical properties by the reduced temperatures afforded by the dry pressure-oxidation of silicon.

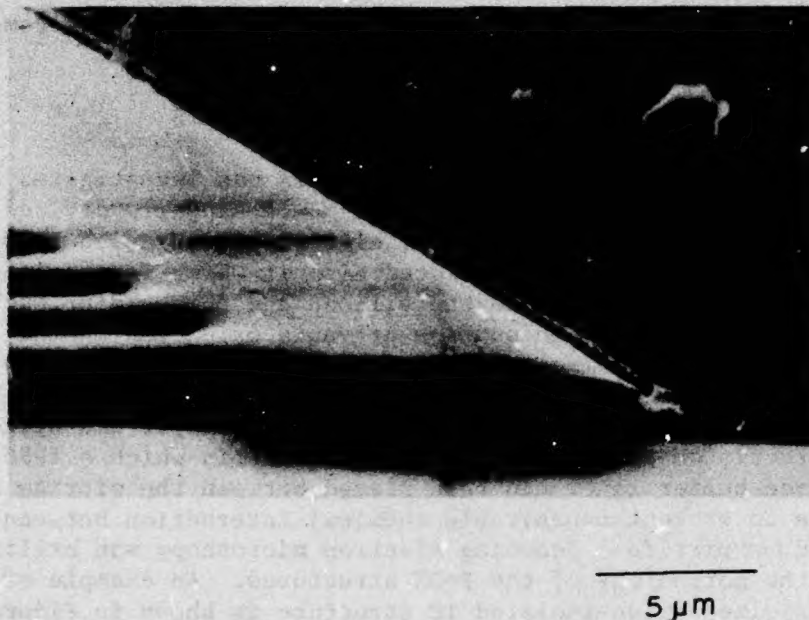
The small flat-band shifts under bias-temperature stress are indicative of a very low level of contamination from alkali and heavy metal ions. Incorporation of such impurities in the growing oxide generally arises from high temperature volatilization in the furnace environment. Reduced volatilization of components in the oxidation furnace is expected at the lower temperatures used for P-OX; for example, the 1 atm boiling point of sodium is about 880°C. Improved oxide stoichiometry, and thus dielectric strength, may also be anticipated by reason of reduced oxide dissociation at the lower temperatures involved in P-OX. Pressure oxides were examined by electron spin resonance and revealed the relative absence of defects compared to oxides prepared by conventional oxidation methods (8). All of these results serve to verify the original program rationale of using

pressure to accelerate oxide growth, obtain lower oxidation temperatures, reduce defects, and improve electrical properties.

#### OXIDE-ISOLATED INTEGRATED CIRCUITS

The application of P-OX to IC structures was investigated for oxide isolation in bulk silicon and silicon-on-sapphire devices (9). According to this type of IC process, electrical isolation between individual components on an integrated circuit wafer is achieved by a deep oxidation extending into the silicon and surrounding each device. A nitride mask on the surface prevents oxidation in the areas where the components themselves are to be fabricated (10). For the P-OX experiments two types of IC structures were examined, one in which a 2000 Å silicon nitride oxidation masking layer had been deposited directly on the silicon surface and one in which a 1000 Å thermal oxide buffer layer had been placed between the nitride and the surface to prevent undesirable chemical interaction between the silicon and the nitride. Scanning electron microscopy was utilized to reveal the morphology of the P-OX structures. An example of a pressure-oxidized oxide-isolated IC structure is shown in Figure 3 for an SOS nitride-on-silicon structure. In Figure 3 the oxide extends completely through the 1 micrometer epitaxial silicon layer of the SOS structure, thus effecting dielectric isolation of adjacent silicon elements. In this particular case, the oxide was prepared by 23-hour P-OX at 850°C, 250 atm dry oxygen, but a more optimum set of conditions can be chosen. Following the P-OX treatment the structures were well defined, and there were no cracks in the nitride films or silicon substrates. Furthermore, it was found in additional experiments that the nitride mask was relatively unattacked, even at dry oxygen pressures to 500 atm. A 44-hour experiment at 825°C, 500 atm resulted in less than 100 Å oxidation of silicon nitride.

Several distinct advantages are apparent for P-OX compared to the 1 atm wet oxidation method used for oxide isolation. First, reduction of the oxidation temperature to 850°C, from the conventionally used 1000°C (10), diminishes and may prevent alteration of the desired silicon dopant concentrations that control device properties. These required dopant concentrations are achieved in the silicon by diffusion processes prior to oxidation. At high oxidation temperatures such as 1000°C, the dopants redistribute via continued diffusion, with consequent alteration of device properties. Thus P-OX may improve device performance, yield, cost, and reliability. Second, it appears possible that the oxide buffer layer under the nitride can be eliminated, thereby reducing lateral oxidation underneath the mask and improving the packing density of oxide-isolated IC device structures. The extent of lateral oxidation underneath the nitride



**Figure 3. Dry pressure-oxidation of nitride on 1 micrometer (100) SOS structure showing 2.2 micrometer pressure-oxide (light) and masking nitride (dark) with complete oxide-isolation between the silicon areas under the nitride.**

mask has an important bearing on device design since lateral oxidation establishes a minimum size for the separation of adjacent isolated structures. Although lateral oxidation is much more extensive in the presence of the intermediate oxide layer (11), this layer is needed for the high temperature wet oxidation method to prevent severe dislocation damage in the silicon. For P-OX, lateral oxidation underneath the nitride mask was negligible and the use of a chromate etch failed to reveal significant nitride induced dislocations in the underlying silicon. Thus low temperature P-OX may satisfactorily reduce the nitride/silicon thermal expansion mismatch so that the intermediate oxide layer may not be needed. On the basis of these results, a joint device/research program is currently being conducted incorporating P-OX in the processing of a working SOS device.



## FUTURE PLANS

A result of the demonstrated merits of dry pressure-oxidation is the intent of ARPA to provide funds to foster industrial utilization of the technique. Apparatus for the processing of 2- or 3-inch diameter wafers is not presently available, and scale-up of the apparatus used in our work is not practical in terms of IC device processing. With our experience in P-OX, pressure, and IC technology, we are designing an internally heated, externally cooled pressure vessel for operation at temperatures to 900°C simultaneous with pressures to 500 atm. Based on metallurgical properties, the vessel would have virtually infinite lifetime at these conditions and adequate operating safeguards. The program is planned to start in FY 77 and will be directed at the fabrication of the apparatus and its use and evaluation for IC device processing. Several industrial and academic organizations have inquired about the availability of apparatus to initiate programs using P-OX. In the current absence of suitable apparatus, we are considering several cooperative efforts in which we will provide P-OX samples, both for evaluation of ICs and for research studies.

From the knowledge gained by our studies of P-OX with semiconductor silicon, other semiconductors used in electronic devices were considered where P-OX might prove beneficial. A class of such materials consists of the III-V compound and alloy semiconductors. The passivation of these semiconductors is a serious barrier problem affecting their current and potential use. Passivation is presently achieved by either deposited oxides or anodic oxidation. These methods are not as desirable as thermally grown oxides in terms of interface properties and oxide density. Native oxides of III-V semiconductors cannot be grown due to the high vapor pressures of the components and loss of stoichiometry by high temperature volatilization. It is anticipated that reduced temperature, high pressure P-OX may alleviate this problem and permit the native oxide passivation of III-V compound and alloy semiconductors. A research program on this subject is scheduled to begin this year.

## CONCLUSIONS

The following conclusions resulted from this study:

1. The thermal oxidation of silicon is significantly accelerated by elevated, but practical, dry oxygen pressures such as 140 atm (2060 psi). Oxide growth by 140 atm P-OX is faster than 1 atm steam oxidation at 800°C.

2. Thermal oxidation temperatures of silicon are reduced as much as 400°C by the use of only about 2000 psi dry oxygen pressure.
3. Gate, field, and isolation oxides for a wide range of silicon integrated circuit devices can be prepared at reduced temperatures and times by dry pressure-oxidation.
4. The mechanism of thermal oxidation of silicon is altered by dry oxygen pressures above 1 atm.
5. The MOS properties of dry pressure oxides are equal or superior to those of conventionally prepared thermal oxides.
6. Silicon nitride is a stable oxidation mask at dry oxygen pressures to 500 atm, permitting the application of P-OX to oxide isolated integrated circuits and SOS technology.
7. The method of pressure-oxidation is suitable for industrial utilization for the processing of silicon integrated circuit devices.
8. Pressure-oxidation is a new passivation technique that has potential merit for semiconductors other than silicon, e.g., the passivation of III-V compound and alloy semiconductors.

#### ACKNOWLEDGMENTS

The authors gratefully acknowledge the specific efforts of S. Marshall in the preparation of SOS wafers for demonstration of pressure-oxidation of IC structures. The authors are also grateful to S. Marshall and G.J. Iafrate for helpful discussions and suggestions, E. Kostyk for MOS metallizations, and C. Cook for scanning electron microscopy analysis. Part of this work was supported from Independent Laboratory In-House Research (ILIR) funds.

#### REFERENCES

1. R.J. Zeto, C.G. Thornton, E. Hryckowian, and C.D. Bosco, "Low Temperature Thermal Oxidation of Silicon by Dry Oxygen Pressure Above 1 Atm," J. Electrochem. Soc. 122, 1409 (1975).
2. J.R. Ligenza, "Oxidation of Silicon by High-Pressure Steam," J. Electrochem. Soc. 109, 73 (1962).
3. B.E. Deal and A.S. Grove, "General Relationship for the Thermal Oxidation of Silicon," J. Appl. Phys. 36, 3770 (1965).
4. B.E. Deal, Private communication.
5. J.R. Ligenza, Private communication.
6. R.J. Zeto, E. Hryckowian, and C.D. Bosco, "New Class of Materials for High Energy Storage Applications from Crystallization of Inorganic Dielectric Glasses Under Pressure," presented at the Army Science Conference, West Point, N.Y., June, 1972.
7. "Integrated Silicon Device Technology, Volume VIII: Oxidation," Research Triangle Institute, Durham, North Carolina, 49 (1965).
8. P.J. Caplan, J.N. Helbert, B.E. Wagner, and E.H. Poindexter, "Paramagnetic Defects in Silicon/Silicon Dioxide Systems," Surface Science 54, 33 (1976).
9. S. Marshall, R.J. Zeto, and C.G. Thornton, "Dry Pressure Local Oxidation of Silicon for IC Isolation," J. Electrochem. Soc. 122, 1411 (1975).
10. J.A. Appels, E. Kooi, M.M. Paffen, J.J.H. Schatorje, and W.H.C.G. Verkuylen, "Local Oxidation of Silicon and Its Application in Semiconductor-Device Technology," Philips Res. Repts. 25, 118 (1970).
11. J.A. Appels and M.M. Paffen, "Local Oxidation of Silicon; New Technological Aspects," Philips Res. Repts. 26, 157 (1971).